TRUETIME

Model 560-5181-3
WIDE BAND ANALOG PRIMARY-SECONDARY SWITCH/DRIVER

SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5181-3 card is configured to provide the user six analog outputs. A variable amplifier (front panel control) connects to six analog output buffers that can drive 50 ohm loads. The six outputs connect through the backplane connector and are delivered to external cables via the I/O card installed in the rear slot directly behind the 560-5181-3 card.

The signal source for the card is one of the timing signals that is distributed via INPUT 1 through INPUT 8 on the Model 56000 backplane. The card is configured at installation by DIP switches to select the signal that will be the Primary and Secondary input.

The Primary and Secondary inputs are monitored for activity. The activity on both inputs is compared to the Delay switch time-out setting (user settable DIP switch SW3) which operates as a watch dog timer. If activity on either the Primary or the Secondary inputs exceeds the delay switch time-out setting, that input is considered bad. NOTE: An input may be considered bad if the minimum input voltage level is not met.

The 560-5181-3 card can operate without a Fault Monitor CPU card installed in the system. In a system without CPU card, the 560-5181-3 card will automatically switch to the Secondary input source when the following conditions are met:

1. The Secondary input is good (activity time-out not exceeded).
2. The Primary input is bad (activity time-out exceeded).

The card will not switch to the Secondary input source if it has been detected bad. The card will switch back to the Primary input signal source only after the Primary input has been qualified good (good for 1 to 2 minutes). This feature restores the card to normal operation automatically.

When a CPU card is installed in the system, the 560-5181-3 card is monitored and can also be controlled by the CPU card. In addition to the 560-5181-3 on-card automatic Primary to Secondary switch-over, the CPU card also provides Primary to Secondary input switching when the CPU detects a Primary Status Input fault. The CPU control provides what is called a “Bank Switch” meaning that all cards in the system will switch from the Primary to the Secondary signal source and will stay on the Secondary input until the user commands a switch to Primary via the CPU card. The “Bank Switch” allows timing signal inputs on all cards installed in the system to come from one source. The CPU also has the ability (under user control) to force the use of either the Primary or Secondary inputs.

1.2 FAULT LINE TRANSCEIVER FUNCTION

This is a serial half-duplex signaling operation between the 560-5181-3 card and the Fault Monitor CPU via the active-low FAULT signal line. The Fault Monitor CPU sends control and switching information to the 560-5181-3 assembly serially. The 560-5181-3 assembly provides status information serially to the Fault Monitor CPU.

1.3 PRIMARY/ SECONDARY SIGNAL SELECT FUNCTIONS

If the 560-5181-3 is operating using the Primary input signal and it detects inactivity on this input, the 560-5181-3 card will automatically or, under Fault Monitor CPU control, switch to the Secondary input signal. If the 560-5181-3 card is operating in a system with a Fault Monitor CPU card and the 560-5181-3 card has switched to the Secondary input source, the 560-5181-3 card will NOT switch back to the Primary input unless commanded by the user via the Fault Monitor CPU.

1.4 PHYSICAL SPECIFICATIONS

Dimensions:	0.8”w X 3.94”h X 8.66”d (2 cm X 10 cm X 22 cm)
Weight:	Approximately ½ pound (¼ kg)

1.5 ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection
Altitude:	10,000 ft. ASL

1.6 POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	4 W (all six outputs driving 50 ohm loads)

1.7 FUNCTIONAL SPECIFICATIONS

1.7.1 INPUT 1 THROUGH 8

Analog Input Level:	2-5 Vpp
Impedance:	>20k ohms
Frequency:	DC to 5 MHz

1.7.2 ANALOG OUTPUTS

Quantity:	6
Signal Type:	Analog
Amplitude:	0 to 3 Vpp into 50 ohms, adjustable
Signal Delay:	< 350 ns

1.7.3 DRC CARD COMPATIBILITY

Location:	Slot 1-17 with compatible I/O card in rear slot.
Compatibility:	See Card Compatibility Matrix.

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

All cards, input cables and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events.

Typically, adjacent-card hot swapping has a negligible effect on the Analog output card. The effect of redundant power supply switch-over is also negligible.

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5181-3 analog output card involves selection of the following DIP switches:

1. 560-5181-3 required settings (SW4 & SW7)
2. Primary input signal switch (SW5)
3. Secondary input signal switch (SW6)
4. Primary input enable switch (SW1)
5. Secondary input enable switch (SW2)
6. Delay switch (activity time-out) (SW3)
7. Delay switch (output faults) (SW3)

2.3.1 560-5181-3 REQUIRED SETTINGS (SW4 & SW7)

SW4 and SW7 MUST be set as follows:
SW4 switches 1 through 8 = ON
SW7 switches 1 through 8 = OFF

2.3.2 PRIMARY INPUT SOURCE SWITCH (SW5)

Set one SW5 switch to the ON position. The SW5 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.3 SECONDARY INPUT SOURCE SWITCH (SW6)

Set one SW6 switch to the ON position. The SW6 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.4 PRIMARY INPUT ENABLE SWITCH (SW1)

This switch MUST be set to a binary representation of the SW5 setting, the Primary input signal switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

PRIMARY INPUT	SW1-1	SW1-2	SW1-3	SW1-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Primary input. If SW1 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Primary input.

2.3.5 SECONDARY INPUT ENABLE SWITCH (SW2)

This switch MUST be set to a binary representation of the SW6 setting, the Secondary input signal switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

SECONDARY INPUT	SW2-1	SW2-2	SW2-3	SW2-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Secondary input. If SW2 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Secondary input.

2.3.6 DELAY SWITCH (Activity Time-Out SW3 Switches 1, 2, & 3)

SW3 switches 1 through 3 are used to set the input activity time-out delay. The user should set the delay for a time-out value that is the closest to but longer than the period of the input signal. This will provide fault detection in the shortest amount of time (Primary to Secondary switch-over time is minimized).

Example Setting: If the input signal is 1 kHz (1 millisecond period), the appropriate setting would be SW3-1 ON, SW3-2 OFF, SW3-3 OFF --(2.048 millisecond time-out).

DELAY (TIME-OUT)	SW3-1	SW3-2	SW3-3
204.8 microseconds	OFF	OFF	OFF
2.048 milliseconds	ON	OFF	OFF
20.48 milliseconds	OFF	ON	OFF
204.8 milliseconds	ON	ON	OFF
2.048 seconds	OFF	OFF	ON
20.48 seconds	ON	OFF	ON
122.88 seconds	OFF	ON	ON
Infinite	ON	ON	ON

If infinite delay has been selected, Primary and Secondary input fault detection is disabled.

2.3.7 DELAY SWITCH (Output Fault Detection SW3-4)

SW3 switch 4 is used to enable or disable output fault detection. If the switch is ON, output fault reporting is disabled. The front panel output fault status LEDs are disabled (off) and output fault reporting to the CPU will cease. This can be used when the user

adjustable output voltage level has been set to a level less than the fixed detection level.

2.4 FAULT STATUS INDICATIONS

All LED indicators activate briefly following hot-insertion or power-up. The following paragraphs describe operation during steady-state conditions.

2.4.1 P/S FAULT INDICATOR

P/S = Primary/Secondary. The P/S indicator provides a visual indication of Primary and Secondary signal loss. If the Primary and the Secondary inputs are lost, the P/S LED will blink at a once per second rate (approx.). A solid ON P/S LED indicates a local power supply failure.

2.4.2 OUT FAULT INDICATORS

The OUT A through OUT F fault indicators activate when the associated output drivers have failed. Note that the detector is designed to detect failed drivers and, typically, will not detect a shorted output.

2.4.3 INIT. FAULT INDICATOR

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.4.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5181-3 card status. This status is available via the Fault Monitor CPU serial port. When it is presented in a 2-byte format, with individual bit definitions as follows:

FAULT STATUS 0	BIT	STATUS (1=ACTIVE)
Low	0	Output Fault A*
Nibble	1	Output Fault B*
Low	2	Output Fault C*
Byte	3	Output Fault D*
High	4	Output Fault E*
Nibble	5	Output Fault F*
Low	6	Not Defined
Byte	7	Not Defined
FAULT STATUS 1	**BIT**	**STATUS (1=ACTIVE)**
Low	0	Power Cycled
Nibble	1	Primary Input Inactive*
High	2	Secondary Input Inactive*
Byte	3	Source = Primary
High	4	Not Defined
Nibble	5	Not Defined
High	6	Not Defined
Byte	7	Not Defined

STATUS REG 0	BIT	STATUS (1=ACTIVE)
Low	0	Pri Input Enable SW1-1
Nibble	1	Pri Input Enable SW1-2
Low	2	Pri Input Enable SW1-3
Byte	3	Pri Input Enable SW1-4
High	4	Sec Input Enable SW2-1
Nibble	5	Sec Input Enable SW2-2
Low	6	Sec Input Enable SW2-3
Byte	7	Sec Input Enable SW2-4
STATUS REG 1	**BIT**	**STATUS (1=ACTIVE)**
Low	0	Delay SW3-1
Nibble	1	Delay SW3-2
High	2	Delay SW3-3
Byte	3	Output Faults OFF
High	4	Always 1 (Analog)
Nibble	5	Always 0
High	6	Not Defined
Byte	7	Not Defined

* Latched fault bit--reset via Fault Monitor CPU.

560-5181-3 CARD ID: 0x0013

SECTION THREE

3 THEORY OF OPERATION

3.1 GENERAL INFORMATION

This section contains a detailed description of the circuits in the 560-5181-3 Analog Output card. Use these descriptions in conjunction with the drawings in SECTION FOUR.

3.2 HARDWARE DESCRIPTION

The 560-5181-3 Analog Output card incorporates Primary and Secondary signal input source switches, a DC-to-DC Converter, a user adjustable output level (front panel) control, six analog 50 ohm output drivers, Input and Output fault-detection circuitry and 7 Fault Indicators.

3.3 DETAILED DESCRIPTION

Reference drawing 560-5181.

3.3.1 PRIMARY & SECONDARY INPUTS (Sheet 6)

SW5 is the Primary Input select switch. One of the eight switches should be in the ON position. This switch directs the signal on backplane INPUT 1 through INPUT 8 to a voltage follower (buffer) and then to an analog multiplexer. SW6 is the Secondary Input select switch. One of the eight switches should be in the ON position. This switch directs the signal on backplane INPUT 1 through INPUT 8 to a buffer and then to an analog switch. The output from the analog switch (either from the Primary or Secondary input) connects to the front panel output amplitude pot.

The signals from the Primary and Secondary inputs are also compared to a fixed voltage reference using two voltage comparators. NOTE: The input voltage level on the Primary and Secondary inputs must meet the minimum input voltage specifications or the input activity detection circuitry will indicate a loss of signal.

The output of the Primary and Secondary comparators connect to a Field Programmable Gate Array (FPGA) which monitors the inputs for activity. If both the Primary and Secondary inputs are detected bad, the front panel P/S fault status LED will blink at a once per second rate. This indicates that the Analog output card does not have a viable input signal source.

3.3.2 ANALOG OUTPUTS (Sheet 5)

The front panel output level control pot connects to an amplifier which provides a fixed gain of 3. The analog output from this amplifier connects to six analog 50 ohm output buffers. These

analog buffers are connected through analog output switch SW4 to the backplane connector P1.

3.3.3 POWER SUPPLY (Sheet 7)

The DC-to-DC Converter converts 48 VDC backplane power to local ±5 VDC power. It is fully-isolated from the backplane power and referenced to signal GND on the Analog output card. Backplane power is supplied via a Polyswitch fuse device, diode and Pi-section L-C filter. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode and L-C filter serve a triple purpose. During live-insertion, the high-current inductor minimizes in-rush current to the DC-to-DC being inserted; and, the diode and capacitor serve to hold up the local voltage at the input to each currently-installed DC-to-DC. During steady-state conditions, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC side of the supply is artificially loaded, providing a minimum load to improve output voltage regulation. The power-up reset generator, assures that RESET is active while the +5 VDC supply is between 1 and 4.5 VDC. This guarantees proper configuration of the Xilinx FPGA during hot swapping and power-up.

3.3.4 FPGA (Sheet 4)

The Field Programmable Gate Array (FPGA) is the interface between the Analog output card and the CPU (if installed). The FPGA provides the timing and control signals for the Analog output card in both local and CPU operating modes.

3.3.5 FAULT DETECTION (Sheets 4 & 6)

There are two categories of fault detection: Input signal faults and Output driver faults. Both use a combination of discrete components and Xilinx FPGA logic to perform the detection task.

Input signal faults are described in paragraph 3.3.1 “Primary & Secondary Inputs”. The output driver fault detector consists of a 1 of 8 analog multiplexer that samples the 6 analog outputs under the control of the FPGA. The multiplexer switches from output to output at rate determined by the Delay switch (SW3) setting. The output being sampled by the analog multiplexer is compared to a fixed reference voltage with a voltage comparator.

The output from the voltage comparator connects to the FPGA which operates internal watchdog timers that monitor activity on the six analog output signals. The watchdog timer time-out is based on the Delay switch setting (SW3). If the watchdog timer on a given output times out, the FPGA recognizes this as an output signal fault and activates the appropriate front panel LED fault indicator.

3.3.6 BACKPLANE FAULT OUTPUT

Inside the FPGA, all faults are combined to form a composite fault signal which is used to drive the Fault line to the Fault Monitor CPU. Fault-signal active indicates status-bit true. (Note that FAULT signal is active-low on the backplane.) Refer to manual section 2.4.4 for detailed information on the fault reporting.

3.3.7 FAULT INDICATORS (Sheet 7)

The INIT. FAULT indicator is driven by the FPGA Initialization-done signal. It activates during initialization, and remains active if initialization does not complete. This is an extremely unusual occurrence.

The P/S FAULT indicator is powered directly from the backplane 48 VDC power buss and is controlled via an opto-isolator to maintain 48 VDC isolation. If local 5 VDC power is lost, the P/S indicator will be ON. The P/S indicator is held off by the Primary/Secondary input fault detection logic. When either of the input signal sources are viable, the indicator will be OFF. When both Primary and Secondary inputs are detected bad, the P/S FAULT indicator will blink ON and OFF.

The OUT fault indicators are controlled directly by the fault detection logic.

SECTION FOUR

4. DETAILED DRAWINGS

4.1	560-5181	DETAILED DRAWINGS
4.2	560-5181-3	BILL OF MATERIALS